Laboratory 3

(Due date: **002**: February 16th, **003**: February 17th, **004**: February 18th)

OBJECTIVES

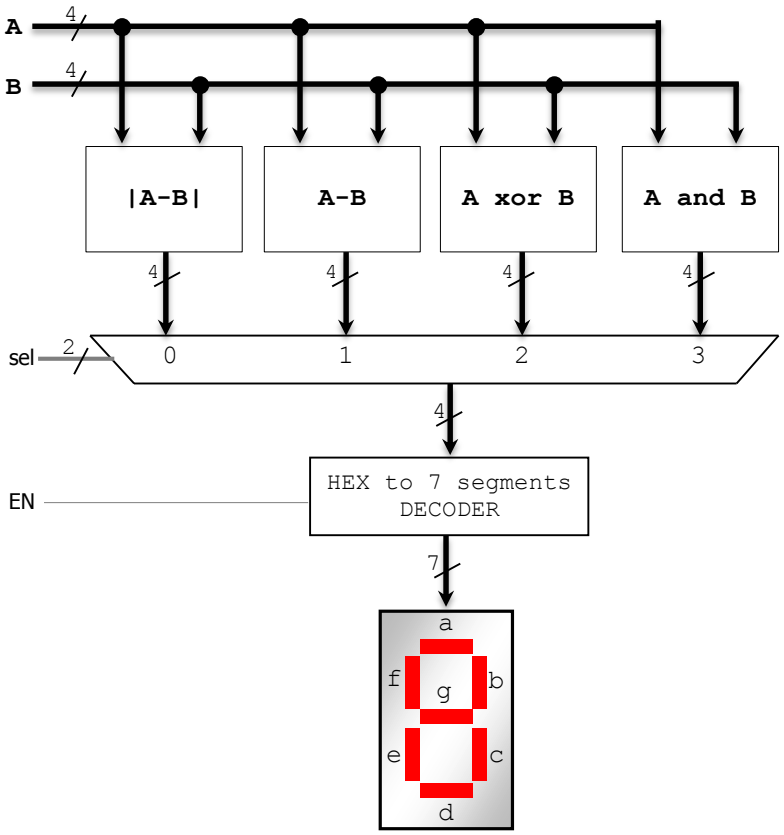
- ✓ Use the Concurrent Description and the Structural Description in VHDL.
- ✓ Implement Combinational circuits on an FPGA.

VHDL CODING

- ✓ Refer to the Tutorial: VHDL for FPGAs for a list of examples.

FIRST ACTIVITY (100/100)

- **PROBLEM:** The following circuit selects between arithmetic (absolute value, subtraction) and logical (XOR, AND) operations.
- Only one result (hexadecimal value) can be shown on the 7-segment display. This is selected by the input `sel(1..0)`.
- Input `EN`: If `EN=1`, the result is shown on the 7-segment display. If `EN=0`, all LEDs in the 7-segment display are off.
- Inputs `A` and `B`: 4-bit unsigned numbers.
- `A-B`: If there is a borrow out, ignore it.
- `|A-B|`: Note that the result only requires 4 bits.
- `A xor B`, `A and B`: These are bit-wise operations.
- **Nexys-4**: Each 7-segment display has an enable input. You must make sure that only one 7-segment is activated.



- ✓ Create a new ISE Project. Select the **XC7A100T-1CSG324 Artix-7 FPGA** device.
- ✓ Write the VHDL code for the given circuit. To implement the arithmetic circuits (`A-B` and `|A-B|`), use full adders (or full subtractors) and logic gates. To implement the Bus MUX and decoder, it is strongly advised that you use the VHDL concurrent statements. To implement the top file, use the Structural Description: Create a separate file for the Arithmetic and Logic circuits, the 4-to-1 Bus MUX, and the Hex to 7-segment decoder.
- ✓ Write the VHDL testbench to test the circuit to test representative cases (or all cases).
- ✓ Perform Functional Simulation and Timing Simulation of your design. **Demonstrate this to your TA**.
- ✓ I/O Assignment: Create the UCF file. Nexys-4: Use SW0 to SW7 for the inputs A and B, and the 7-segment display for the output. For the inputs `sel` and `EN`, you can use SW8 to SW10, or you can use the push buttons.
- ✓ Generate and download the bitstream on the FPGA and test. **Demonstrate this to your TA**.

- Submit (as a .zip file) all the generated files: VHDL code files, VHDL testbench, and UCF file to Moodle (an assignment will be created). DO NOT submit the whole ISE Project.

TA signature: _____ **Date:** _____

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